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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,951	01/20/2004	Michael Peter Mortensen	200209111-1	1445

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,951	MORTENSEN ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 01/20/2004. Claims 1-24 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-2, 4, 11-12, 14, 21-22, and 23-24 are** rejected under 35 U.S.C. 102(b) as being anticipated by **Abato et al. (US Patent No. 5,508,937).**

3. **Referring to claim 1 and similarly recited claims 11, 21, and 23,** Abato et al. disclose a method comprising: receiving circuit analysis results;

identifying a duplicate circuit analysis result among the received circuit analysis results (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting , a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")); and

outputting a list of circuit analysis results that excludes the duplicate circuit analysis result (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")).

4. **Referring to claim 2 and similarly recited claim 12,** Abato et al. disclose the method of claim 1, further comprising:

sorting the circuit analysis results (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")).

5. **Referring to claim 4 and similarly recited claim 14**, Abato et al. disclose the method of claim 2, further comprising:

comparing each of the circuit analysis results with an adjacent circuit analysis result (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")).

6. **Referring to claim 22**, Abato et al. disclose the computer readable medium of claim 1, wherein the computer-readable instructions are further configured to:

sort the circuit analysis results (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")); and

compare each of the circuit analysis results with an adjacent circuit analysis result (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")).

7. **Referring to claim 24,** Abato et al. disclose the system of claim 23, further comprising:

means for sorting the circuit analysis results (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")); and

means for comparing each of the circuit analysis results with an adjacent circuit analysis result (col. 10, ll. 30-46, disclose a step of sorting, i.e. includes identifying and outputting steps, a recalculation list to eliminate unnecessary recalculation of the same values (i.e. "duplicate analysis results")).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 3 and similarly recited claim 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al. in view of Beausang et al. (US Patent No. 6106568).

Abato et al. disclose the limitations in claims 1 and 2 except wherein the circuit analysis results are sorted alphabetically.

Beausang et al. disclose a hierarchical scan architecture design method (see abstract) includes an analysis method wherein the circuit analysis results are sorted alphabetically (page 13 , ll. 50-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Abato et al. with the method disclosed by Beausang et al. because such modification includes an analysis results which are

sorted alphabetically to thereby provide an efficient method for architecting design for test circuitry (abstract; col. 2, ll. 61-col. 3, ll. 14).

10. **Claims 5-10 and 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al. in view of Chandra et al. (US Patent No. 6591402).

11. **Referring to claim 5 and similarly recited claim 15**, Abato et al. the method of claim 2 except wherein the circuit analysis results are sorted based on types of circuit analysis results.

Chandra et al. disclose a system and method for analyzing assertion-based circuit designs wherein the circuit analysis results are sorted based on types of circuit analysis results (abstract; col. 8, ll. 31-col. 9, ll. 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Abato et al. with the method disclosed by Chandra et al. because such modification includes an analysis results which are sorted based on types of analysis results to thereby provide an efficient method for analyzing circuit designs which increases the predictability of the circuit design (col. 3, ll. 19-35).

12. **Referring to claim 6 and similarly recited claim 16**, Chandra et al. further disclose the method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of latch design defects (col. 10, ll. 18-41, see "latches", "violation", and "sorted").

13. **Referring to claim 7 and similarly recited claim 17**, Chandra et al. further disclose the method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of dynamic gate design defects (col. 23, ll. 20-col. 24, ll. 44).

14. **Referring to claim 8 and similarly recited claim 18**, Chandra et al. further disclose the method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of clock design defects (col. 10, ll. 18-41; table 3).

15. **Referring to claim 9 and similarly recited claim 19**, Chandra et al. further disclose the method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pseudo-NMOS gate design defects (see tables 1-2).

16. **Referring to claim 10 and similarly recited claim 20**, Chandra et al. further disclose the method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pass-FET design defects (See table 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
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PRIMARY EXAMINER